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A COMPLETE SMALL SIZE 2 TO 30 GHz HYBRID DISTRIBUTED AMPLIFIER USING A NOVEL DESIGN TECHNIQUE

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Summary

A 2-30 GHz hybrid distributed amplifier has been designed using a novel design technique. It includes the bias circuitries and exhibits 4.8 dB ± 0.4 dB up to 30 GHz. The design approach is based on a detailed analysis of the impedances and the cut-off frequency of the transmission lines to reduce the ripple and to increase the bandwith. This novel approach can be applied in order to improve more generally the performance of distributed amplifiers.

This is the first hybrid amplifier ever reported to cover such a wide frequency range using 0.5 µm GaAs FETs and including the bias circuitries.

Introduction

The wide bandwidth capability of distributed amplifiers is well known (1) - (5). However, recent improvements in GaAs FET and monolithic circuits technologies have created new prospects in wideband amplification up to 40 GHz (6). In distributed amplification, active devices are combined with microstrip lines to form two coupled artificial transmission lines. The conditions on the phase velocity and characteristic impedances enable the achievement of gain over a large bandwidth. In the conventional approach, the cut-off frequency and the characteristic impedance of the transmission lines are fixed through the FET capacitances. Taking into account the losses of the drain and gate lines, due to the transistor parasitic elements, the amplifier bandwidth is smaller than that of the ideal transmission lines. Conventional design methods are based on the computation of the optimum number of FET's, while in order to get a flat gain response, a classical alternative is to establish the relationship between the cut-off frequency of the lines and the maximum required operating frequency (5), (7). But these techniques do not allow us to take advantage of the maximum capabilities of the FET's and to increase the gain bandwidth product. The present study focusses on improvements in distributed amplifiers in terms of gain ripple, frequency band and limitations of such amplifiers.

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Detailed analysis of distributed amplifiers

. Origin of the ripple

An important element, causing ripple, is the effect of the gate to drain capacitance of the transistors. This effect appears very quickly and increases when the frequency is increased. The backward waves, generated on the drain line due to the principle of distributed amplification, can be transferred through the Cgd capacitance of the FETs, on the gate line. This signal can be in phase or out of phase with the forward wave and disturb the travelling waves along the lines. Figure 1 shows the effect of Cgd on the gain of the amplifier (bias circuitry included). The coupling effect increases with the frequency causing the ripple. The ripple also finds its origin in the multiple reflections on the loads terminating the artificial transmission lines. This ripple is particularly significant at high frequencies. Due to the gate to drain capacitance of the transistor, the waves generated by these reflections, disturb the travelling waves on both lines.

An other element causing ripple is the drain bias circuitry. Indeed this circuit is also responsible for reflections because of mismatching to the amplifier.

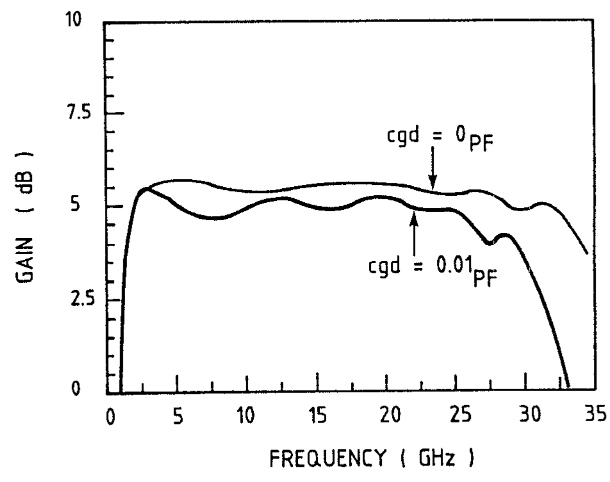

Figure 1
Effect of the gate to drain capacitance of the transistor

. **Frequency limitations**

In distributed amplification, the bandwidth can be limited only by the active devices used. The main condition to obtain this, is to realize strictly the same phase velocity on both lines up to the transmission lines' cut-off frequency. Usually, this cut-off frequency is higher than that of the transistors used.

But the characteristic impedance of the transmission lines is a function of frequency whereas the loads at the idle ports are fixed. Under these conditons, the multiple reflections on the loads increases with the frequency and mismatches the amplifier. These reflections generate backward waves which distrub the travelling waves along the lines.

Figure 2 shows the characteristic impedance of the gate line as a function of frequency. The same behaviour appears on the drain line. The real part of the gate impedance reduces to zero ohms at the cut-off frequency of the line while the imaginary part rises. Above frequency F_b, the amplifier is mismatched, where F_b $F_c/1.7$ which gives VSWR less than 2.

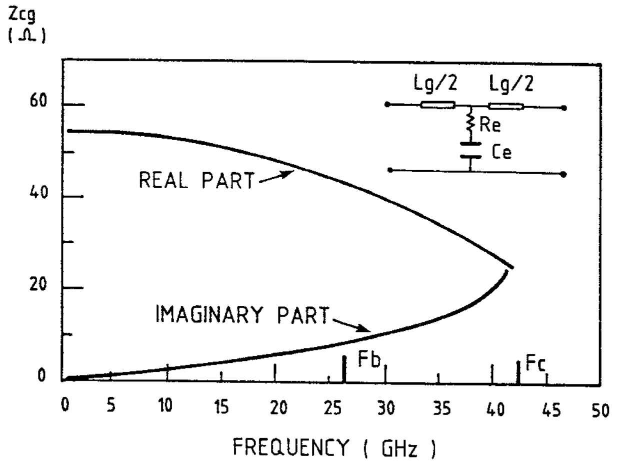

Figure 2
Gate line characteristic impedance versus the frequency

Amplifier improvements

The main problem is to use the FET up to its cut-off frequency. An alternative method is to increase the cut-off frequency F_c of the artificial transmission line far beyond the cut-off frequency of the transistor F_t, this will then mean that there will be flat gain from the amplifier up to F_t. But in order to achieve flat gain up to F_t, the inductances must be reduced (assuming that the FET parameters have not been changed), causing the characteristic impedance of the artificial transmission line to be reduced. This gives rise to matching problems since the expected value of input and output terminations resistance is 50 ohms. The method is based on an good choice of matching circuits at the idle ports in order to realize loads depending on the frequency. These circuits match exactly the transmission lines at their characteristic impedance. The advantages of this approach are to avoid the reflections at the terminations, to reduce the ripple and to use all the maximum bandwidth of the transistor. Figure 3 shows the improvement on the input reflection coefficient at higher frequencies.

Distributed amplifier description

The distributed amplifier circuit configuration is shown in figure 4. The gate and drain capacitive elements of the FET devices are coupled with microstrip lines, forming matched, artificial transmission lines. The amplifier includes the bias circuitry and the matching circuit to realize the frequency dependant load in order to improve the performances. To obtain a high cut-off frequency and optimum gain performances, a GaAs FET, made at LEP (8) with 0.5 µm gate length and 75 µm gate width were required. A photograph of the completed distributed amplifier with 8 sections is shown in figure 5. The circuit is fabricated on 254 µm thick alumina substrate with dimensions of 4 x 6 mm. Both GaAs FET's and decoupling capacitors are soldered on the copper fixture carrying the circuit. The resistances are realized using the adhesion Ni-Cr layer.

Distributed amplifier performances

The gain performance of the amplifier and the I/O VSWR are shown in figure 6. The bias conditions are at $V_{gs} = -0.3$ V, $V_{DS} = 4$ V.

Over the 2 to 29 GHz band, the amplifier exhibits 4.8 ± 0.4 dB gain This was measured in two frequency bands : one covering 2

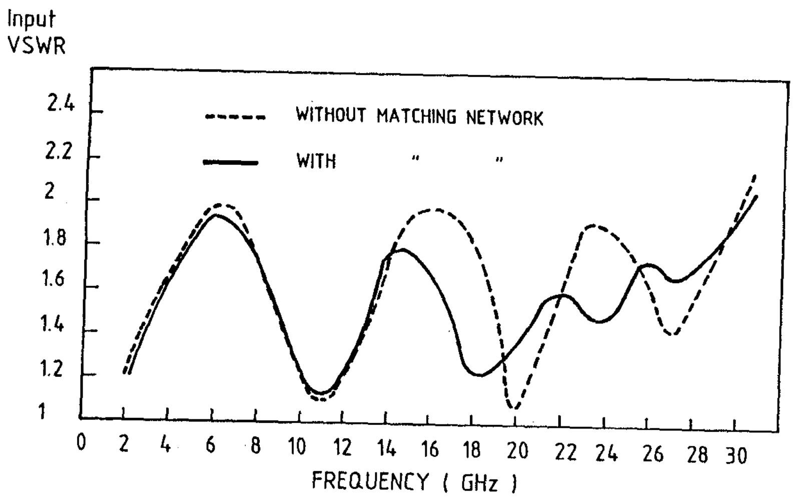

Figure 3
Input VSWR of the amplifier

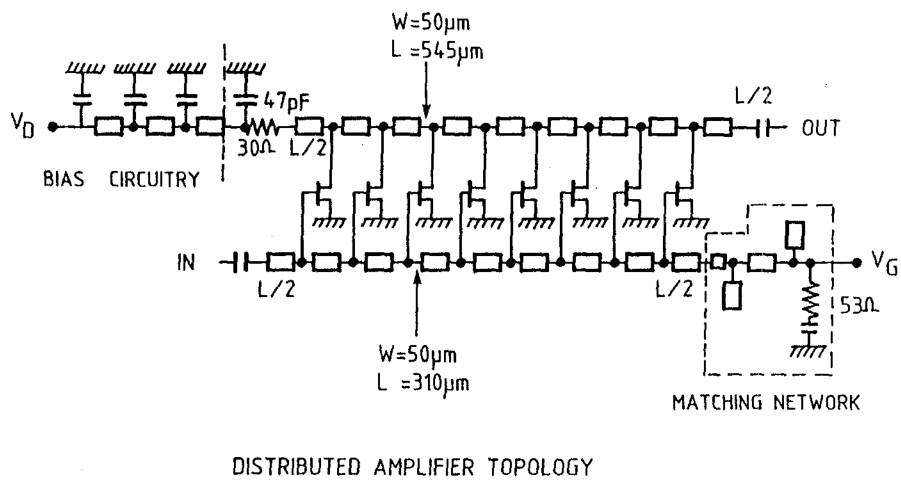

Figure 4
Distributed amplifier topology

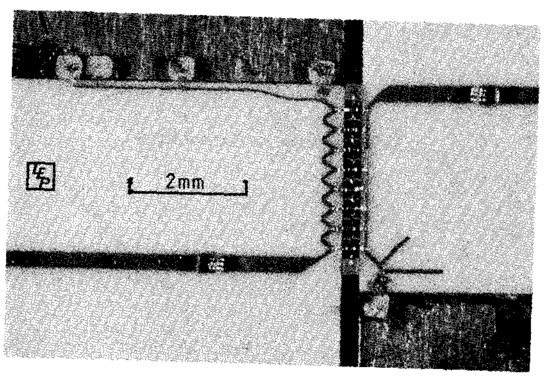

Figure 5
View of the complete amplifier

to 26.5 GHz and the other the 26.5 to 40 GHz.

The noise figure increases from 5 dB at 8 GHz up to 7 dB at 26 GHz.

A good agreement between computed and measured results can be observed.

Conclusion

A complete 2 to 30 GHz hybrid distributed amplifier has been demonstrated up to the K/Ka band frequency range. The amplifier has achieved 4.8 to ± 0.4 dB gain. It appears that hybrid distributed amplifiers can be improved using better parasitic elements handling and a good choice of matching circuits at the idle ports in order to reduce the multiple reflections.

At higher frequencies, the matching network becomes more essential in helping to reduce the magnitude of the reflected waves which are mainly a result of the coupling effect produced by Cgd.

Due to the inherent problems of bonding the active devices to the passive circuit,causing large discontinuities which are hard to model at high frequencies, the MMIC form of technology is more favorable.

Acknowledgements

The author wishes to acknowledge Pierre HUGUET, Michel IOST and André COLLET for fabrication and supply of the FETs. I wish to thank Jean-Christophe MEUNIER for the delicate mounting and measurements.

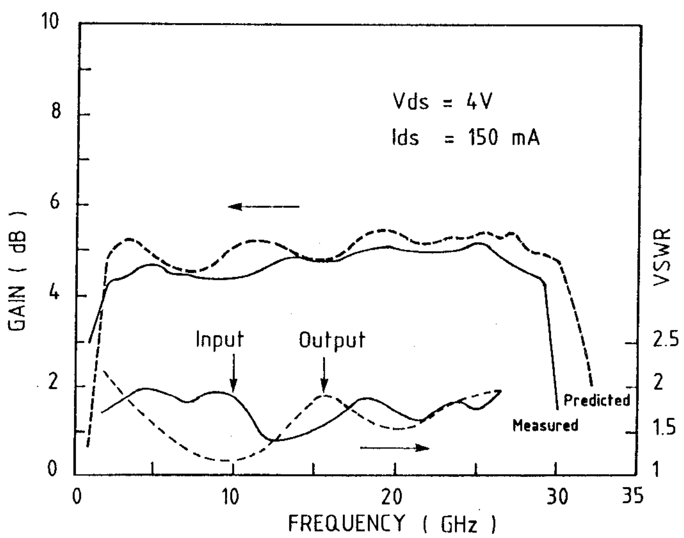

Figure 6
Amplifier performances

References

(1) Y. Ayasli, L.D. Reynolds, R.L. Mozzi, L.K. Hanes
"2-20 GHz GaAs travelling-wave power amplifier", IEEE Trans. on MTT, MTT-32, pp. 290-295, March 1984.

(2) K.B. Niclas, W.T. Wilser, R.T. Kritzer, R.R. Pereira
"On theory and performance of solid-state microwave distributed amplifiers
IEEE Trans. on MTT, MTT-31, pp. 447-456, June 1983.

(3) W. Kennan, T. Andrade, C. Huang
"A miniature 2-18 GHz monolithic GaAs distributed amplifier"
IEEE Monolithic Circuits Symposium, May 1984

(4) B. Kim, H.Q. Tserng
"0.5 W, 2-21 GHz monolithic GaAs distributed amplifier"
Electron. Letters, vol. 20, pp. 288-289, 1984

(5) J.B. Beyer, S.N. Prasad, R.C. Becker, J.E. Wordman, G.K. Hohenwarter
"MESFET distributed amplifier desgin guidelines"
IEEE Trans. on MTT, MTT-32, pp. 268-275, March 1984.

(6) R. Pauley, P. Asher, J.M. Schellenberg H. Yamasaki, P.G. Asher
"A 2 to 40 GHz monolithic distributed amplifier",
GaAs Symposium IC, November 1985

(7) P. Gamand,
"A 0.1 to 25 GHz HMIC distributed amplifier on Al_2O_3 substrate"
15th European Microwave Conference, pp. 541-546, September 1985

(8) P. Huguet, P. Baudet, C. Venet, M. Iost M. Pertus, G. Mennechez
"A 0.5 µm low noise GaAs FET for applications in the Ka-band"
9th European Specialist Workshop on Active Microwave Semiconductors Devices, Veldhoven, Netherlands, October 1984